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Reconfigurable pulse detector in wireless communications system

This invention relates to wireless communications, and in particular to a receiver for use in a wireless communications system. More particularly, the invention relates to a device and a method for pulse detection, for example for use in an Ultra Wideband (UWB) wireless communications system. The communications system may be in the form of

5   a signaling system, in which data is sent from a transmitter to a receiver, or it may be in the form of a radar or positioning system, in which a combined transmitter/receiver detects the reflections of signals which it has itself transmitted.

The term Ultra Wideband is used to refer to a number of different wireless communications systems. In one form of an Ultra Wideband (UWB) communications

10   system, a transmitter generates a series of pulses, which are transmitted at radio frequencies. The function of the receiver is then to detect these pulses, in order to be able to extract data from the transmitted signal.

WO 01/93444 discloses a UWB receiver, for detecting pulses in an incoming signal. The received signal is amplified, and then applied to one input of a mixer. A clock

15   signal is applied to a pulse shaper, which generates a series of local pulses, which may for example be square pulses. These pulses are applied to the other input of the mixer, and multiplied with the received signal.

An integrator then accumulates the mixer output over a predetermined period, and the accumulated output is sampled in an analog-to-digital converter, at a rate that

20   corresponds to a source bit rate. The output of the analog-to-digital converter is then provided to a digital controller for further processing of the received signal.

However, this architecture has the disadvantage that it may take a significant time period for the system to lock on to the new sequence of pulses.

In a possible alternative architecture, the mixer output could be supplied not to

25   an integrator, but to a low–pass filter. Compared with the architecture shown in WO 01/93444, this would have the advantage that the low-pass filter could track the input signal better than the integrator, and so the system would be able to lock faster to a new sequence of pulses. However, it would have the disadvantage that the gain is lower than that of the integrator, and so the achievable signal-noise ratio of the receiver may well be lower.

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According to a first aspect of the present invention, there is provided a receiver architecture, in which the mixer output is applied to a block which can be configured either as an integrator or as a filter.

According to the second aspect of the invention, there is provided a method of operation of such a receiver, in which, when no pulses are being received, the block is configured as a filter, allowing it to lock quickly to any new sequence of pulses, while, when the system has locked to a sequence of pulses, the block is configured as an integrator, so that the improved signal-noise ratio can be achieved.

In the drawings:

Fig. 1 is a block schematic diagram of a wireless communications system in accordance with the present invention.

Fig. 2 is a block schematic diagram of a radio receiver in accordance with an aspect of the present invention.

Fig. 3 is a block schematic diagram showing in more detail the form of the reconfigurable integrator/filter block in a preferred embodiment of the receiver of Fig. 2.

Fig. 4 is a block schematic diagram of an alternative radio receiver in accordance with an aspect of the invention.

Fig. 5 is a block schematic diagram showing the form of the reconfigurable integrator/filter block in a preferred embodiment of the receiver of Fig. 4.

Fig. 6 is a flow chart showing a method of operation of the receiver of Fig. 2 or Fig. 4.

Fig. 1 is a block schematic diagram of a wireless communications system 2, which includes a radio transmitter 6 and a radio receiver 10. In particular, the system is an Ultra Wideband (UWB) wireless communications system, of a type in which signals are transmitted in the form of pulses.

As shown in Fig. 1, the pulses may be transmitted from a separate device 6, for the purpose of transmitting data from that separate device to the receiver 10. Alternatively, the transmitter 6 and receiver 10 may form part of a single device, with the receiver then being used to detect reflections of pulses transmitted from the device, for the purposes of radar or positioning, for example.

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Fig. 2 shows in more detail the form of the receiver 10. Signals are received by an antenna 12, and then amplified in an amplifier 14. The amplified signals are passed to a first input of a mixer 16.

At the same time, a timing generator 18 produces a clock signal, which is
5   applied to a pulse shaper 20.

The pulse shaper 20 generates pulses, in a form which corresponds to the expected shape of received pulses, and this expected shape will depend upon the communications system in which the receiver is to be used. As is generally conventional, the receiver has information about the time positions at which pulses are expected. The timing
10   generator 18 can therefore control the pulse shaper 20 so that the pulses become synchronized with the received signals.

In some situations, the receiver will be used in a communications system in which square pulses are transmitted, while, in other cases, the receiver will be intended for use in a communications system in which other forms of pulse, for example sinusoidal, or
15   part-sinusoidal, pulses, are transmitted.

The pulses, in the shape of the expected received pulses, are then applied to the second input of the mixer 16, in which the received signal is multiplied by the pulses generated in the pulse shaper 20.

The output of the mixer 16 is then supplied to a block 22, which can be
20   configured to act either as an integrator or as a filter, as will be described in more detail below. The block 22 operates under the control of a control signal supplied from a digital signal processor (DSP) 24, which also receives a clock signal from the timing generator 18. The output from the integrator/filter block 22 is supplied to an analog-to-digital converter 26, and the resulting digital signal is supplied on an output line 28, where it can be further
25   processed, for example to retrieve the information content of the received signal in the case of a data transmission system.

Fig. 3 is a schematic diagram, showing a possible form of the integrator/filter block 22 in the receiver 10 of Fig. 2.

The block 22 is based around an operational amplifier 30, the non-inverting
30   input of which is connected to ground, while the inverting input receives the signal output from the mixer 16.

A feedback loop from the output of the operational amplifier 30 to its inverting input contains a capacitor 32, in parallel with a variable resistor 34. The resistor 34 can be

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switched into and out of the loop by means of switches 36, 38, which operate under the control of the control signal supplied from the digital signal processor 24.

When the resistor 34 is out of the feedback loop, the amplifier 30 behaves as an integrator. When the resistor 34 is switched into the feedback loop, the amplifier 30 behaves as a low-pass filter. As shown in Fig. 2, the resistor 34 has a variable resistance value. The resistance value has an effect on the low-frequency gain, and the position of the filter pole, of the low-pass filter. Depending on the noise level which is affecting the received signal, it may be advantageous to vary the low-frequency gain during the period while the receiver is attempting to synchronize to the pulses of the received signal. The resistance value can therefore be adjusted to provide the appropriate level of gain.

Fig. 4 is a block schematic diagram of an alternative form of radio receiver, in accordance with an embodiment of the invention. Again, the receiver 50, shown in Fig. 4, is suitable for detecting pulses transmitted in a UWB wireless communications system. Signals are received by an antenna 52, and then amplified in an amplifier 54. The amplified signals are passed to a first input of a mixer 56.

At the same time, a timing generator 58 produces a clock signal, which is applied to a pulse shaper 60. The pulse shaper 60 generates pulses, in a form which corresponds to the expected shape of received pulses. Again, this expected shape will depend upon the communications system in which the receiver is to be used. These pulses are applied to the second input of the mixer 56, in which the received signal is multiplied by the pulses generated in the pulse shaper 60.

The output of the mixer 56 is then applied to a block 62, which can be configured to act either as an integrator or as a filter, as will be described in more detail below, but which also acts as an analog-to-digital converter. The block 62 operates under the control of a control signal supplied from a digital signal processor (DSP) 64, which also receives a clock signal from the timing generator 58.

The digital signal generated by the block 62 is supplied on an output line 66, where it can be further processed, for example to retrieve the information content of the received signal in the case of a data transmission system.

Fig. 5 is a schematic diagram, showing a possible form of the block 62 in the receiver 50 of Fig. 4.

The block 62, as shown in Fig. 5, is based around a sigma-delta modulator 70 acting as an analog-to-digital converter (ADC). This is a conventional form of ADC, which already includes a filter. As a result, in view of the advantages of this form of ADC, it may be

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more efficient to use an ADC of this form, and also to use the function of the filter within the ADC.

In Fig. 5, it can be seen that the output from the mixer 56 is applied to a first input of a first adder 72, whose output is applied to an integrator 74. The output of the

5   integrator 74 is applied to a first input of a second adder 76, and the output of the adder 76 is applied as an input to the sigma-delta ADC 70.

Specifically, the output from the adder 76 is applied firstly to a low pass filter 78, and then to a quantizer 80, to provide an output on line 66 in digital form.

As is conventional in a sigma-delta ADC, the output from the quantizer 80 is

10   passed back around a feedback loop, firstly being converted back into analog form in a digital-to-analog converter (DAC) 82.

The operation of the feedback loop then depends upon the action of two switches 84, 86, which are controlled by control signals from the DSP 64.

When the first switch 84 is open and the second switch 86 is closed, the

15   received signal is simply applied first to the integrator 74, which acts in a conventional way, and is then applied to the sigma-delta ADC 70, which again operates in a conventional way to convert the signal into digital form.

By contrast, when the first switch 84 is closed and the second switch 86 is open, the integrator 74 appears in the feedback loop.

20   The result in this case is that the block 62 effectively acts as a low pass filter with an analog-to-digital conversion function. More specifically, the block 62 acts as a sigma-delta ADC, in which the order of the low pass filter within the feedback loop has increased by one. The effect of this is small on signals within the signal bandwidth, which occurs at baseband, because the filter has a low-pass characteristic. However, quantization

25   noise generated in the loop is filtered by a higher order filter, and is therefore filtered out more strongly. The result is that the output signal has an improved signal-noise ratio.

The result is that, with the first switch 84 closed and the second switch 86 open, the block 62 is able to lock quickly to a new sequence of pulses received by the antenna 52, while, with the first switch 84 open and the second switch 86 closed, the block 62

30   provides a large gain and hence a good signal-noise ratio.

Fig. 6 is a flow chart showing a method of operation of a receiver in accordance with the invention, and this method can be applied either to the receiver shown in Figs. 2 and 3, or to the receiver shown in Figs. 4 and 5.

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The process starts at step 100, at a time when no pulses are being received. In step 102, the block 22 (in the embodiment of Figs. 2 and 3) or 62 (in the case of the embodiment shown in Figs. 4 and 5) is set to act as a filter. That is, in the case of the embodiment shown in Figs. 2 and 3, a control signal is sent from the digital signal processor 24 to close the switches 36, 38. In the case of the embodiment shown in Figs. 4 and 5, a control signal is sent from the digital signal processor 64 to close the first switch 84 and open the second switch 86.

In step 104, it is then determined whether any received pulses can be detected, and this step repeats until such time as pulses are detected, at which time the process passes to step 106.

In step 106, it is determined whether the receiver has locked on to the received sequence of pulses. This determination can be made by a method which is known to the person skilled in the art, for example as described in WO 00/14910. Step 106 is then repeated until such time as the receiver has locked to the received sequence of pulses. At this time, the process passes to step 108, and the block 22 (in the case of the embodiment shown in Figs. 2 and 3) or 62 (in the case of the embodiment shown in Figs. 4 and 5) is set to act as an integrator.

That is, in the case of the embodiment shown in Figs. 2 and 3, a control signal is sent from the digital signal processor 24 to open the switches 36, 38. In the case of the embodiment shown in Figs. 4 and 5, a control signal is sent from the digital signal processor 64 to open the first switch 84 and close the second switch 86.

Therefore, in the initial acquisition phase, the correlator output is supplied to a filter, to allow fast locking to the received sequence of pulses. Thereafter, during the accumulation phase, the correlator output is supplied to an integrator, which provides a high gain in order to maximize the signal-noise ratio in the received signals, and thereby allow more accurate pulse detection.